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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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ROCKWELL AUTOMATION, INC./BF
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EXAMINER	
PATEL, DHARTI HARIDAS	
ART UNIT	PAPER NUMBER
2836	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/737,226	COVAULT, JACK L.	
	Examiner	Art Unit	
	Dharti H. Patel	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 21-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21-24* is/are allowed.

6)☒ Claim(s) *1-10 and 13* is/are rejected.

7)☒ Claim(s) *11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-2, 4-8, and 13 are rejected under 35 U.S.C. 102(e) as being unpatentable over Poe et al., Patent No. 6,646,847.

With respect to claim 1, Poe teaches a method [Fig. 1 and Fig. 2] for limiting the power consumed by electrical equipment circuits that may be connected to power sources with varying voltages [Col. 2, lines 25-30], that method comprising detecting a magnitude of electric current flowing into the circuits [Fig. 1, 102, or Fig. 2, resistor senses the magnitude of current; Col. 3, lines 9-11] and producing a first signal level [Fig. 1, first input to the voltage sense device 104] that indicates the magnitude of electric current; comparing the first signal level to a reference signal level [Fig. 1, second input to the voltage sense device 104] which comparison produces an output signal [Fig. 1, output coming from 104 and going into control unit 106]; altering one of the first signal level and the reference signal level in response to a determination of voltage applied to the circuits [Abstract, lines 4-11], which results in the output signal

indicating when electric power consumed by the circuits exceeds a threshold level [Fig. 1; when short circuit occurs; Col. 2, lines 25-30]; and disconnecting the power source from the circuits in response to the output signal [Col. 2, lines 30-34]; whereby electrical power is blocked from entering the circuits at a current threshold value that is dependent upon the voltage applied to the circuits [When the short circuit occurs or when the power exceeds a threshold level, drive circuit 112 disconnects load 108 from power supply 114].

With respect to claim 2, Poe teaches that the first signal level and the reference signal level are voltage levels [Fig. 1, Voltage sense device compares two voltages; Col. 3, lines 12-14].

With respect to claim 4, Poe teaches that the altering comprises detecting a load voltage applied to the load to produce a second signal level that indicates the load voltage; and combining the second signal level with the one of the first signal level and the reference signal level [Col. 3, lines 15-58].

With respect to claim 5, Poe teaches that the altering comprises producing a second signal level corresponding to an amount that the load voltage exceeds a defined threshold; and combining the second signal level with the one of the first signal level and the reference signal level [Col. 2, lines 64 – Col. 3, lines 58].

With respect to claim 6, Poe teaches that controlling flow of electric current comprises disconnecting the load from the power source [Col. 2, lines 30-34].

With respect to claim 7, Poe teaches an apparatus [Fig. 1 and Fig. 2] for limiting the power consumed by electrical equipment circuits that may be connected to power sources providing varying voltages [Col. 2, lines 25-30], that apparatus comprising load circuits [Fig. 1, 108] having a designed power limit; input power processing circuits [Fig. 1, consists of 102, 104, 106, and 112] positioned between the load circuits and a power source [Fig. 1, 114], the input power processing circuits including a current sensing circuit [Fig. 1, 102] that detects a magnitude of electric current flowing to the load circuits [Fig. 1, 108] and producing a first signal level that indicates the magnitude of current [Col. 3, lines 9-11]; a comparator [Fig. 1, 104] connected to the current sensing circuit [Fig. 1, 102] and having a first input to which the first signal level [Fig. 1, first input to the voltage sense device 104] is applied, a second input [Fig. 1, second input to the voltage sense device 104] connected to a source of a reference signal level, and a comparator output [Fig. 1, output coming from 104 and going into control unit 106] at which an output signal is produced in response to comparing the first signal level and the reference signal level; a circuit branch [Fig. 1, 110] connected to the comparator [Fig. 1, 104] and which alters one of the first signal level and the reference signal level in response to determination of voltage applied to the load circuits [Abstract, lines 4-11], which results in an output signal indicating when electric power consumed by the load exceeds a threshold level [Fig. 1; when short circuit occurs; Col. 2, lines 25-30]; and a device [Fig. 1, 106] connected to the comparator [Fig. 1, 104] output and

disconnecting flow of electric current from the power source [Fig. 1, 114] to the load circuits [Fig. 1, 108] in response to the output signal [Col. 2, lines 30-34]; whereby electrical power is blocked from entering the load circuits at a current threshold value that is dependent upon the voltage applied to the load circuits to limit power to the load circuits [When the short circuit occurs or when the power exceeds a threshold level, drive circuit 112 disconnects load 108 from power supply 114].

With respect to claim 8, Poe teaches that the first signal level and the reference signal level are voltage levels [Fig. 1, Voltage sense device compares two voltages; Col. 3, lines 12-14].

With respect to claim 13, Poe teaches that the device selectively disconnects the load circuits [Fig. 1, 108] from the power source [Fig. 1, 114] in response to a signal at the comparator output [Col. 2, lines 30-34].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 3 and 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poe et al., Patent No. 6,646,847, in view of Jones et al., Patent No. 6,621,259.

Poe does not disclose that detecting a magnitude of electric current comprising providing current sensing resistor and an operational amplifier. Jones teaches current sense circuit.

With respect to claim 3, Jones teaches that detecting a magnitude of electric current comprises providing current sensing resistor [Fig. 1, 12, Abstract, line 2, Col. 4, lines 12-14] through which electric current flows from the power source [Fig. 1, 14] to the load [Fig. 1, 15], wherein voltage across the current sensing resistor [Fig. 1, 12] indicates a the magnitude of that electric current [Col. 4, lines 28-31]; connecting a first input of an operational amplifier [Fig. 1, 18] to a first side [Fig. 1, 11] of the current sensing resistor [Fig. 1, 12]; and connecting a second input of the operational amplifier [Fig. 1, 18] to a second side [Fig. 1, 13] of the current sensing resistor [Fig. 1, 12][Abstract, lines 1-4, Col. 4, lines 41-43].

Both teachings are analogous current sense circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jones, which teaches a resistor and an operational amplifier, with the current sense circuit of Poe, because the current sense amplifier is more accurate and less expensive, and provides a single output signal indicative of both amplitude and direction of current through the sense resistor.

With respect to claim 9, Jones teaches that the current sensing circuit comprises a current sensing resistor [Fig. 1, 12, Abstract, line 2, Col. 4, lines 12-14], voltage across which indicates the magnitude of current flowing to the load

circuits [Col. 4, lines 28-31]; and an operational amplifier [Fig. 1, 18] having a first input connected to a first side of the current sensing resistor, a second input connected to a second side of the current sensing resistor, and producing the first signal level [Abstract, lines 1-4, Col. 4, lines 41-43].

With respect to claim 10, Jones teaches that the circuit branch comprises an impedance element [Fig. 1, 19] coupling the first input of the comparator [Fig. 1, 18] to one of the first and second sides of the current sensing resistor [Fig. 1, 12, Rsense].

Allowable Subject Matter

3. Claims 11-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 21-24 are allowed.

The following is an examiner's statement of reasons for indicating allowance of claim 11: The prior art does not disclose a second operational amplifier having an input coupled to the circuit element and having a second output connected to the second input of the comparator. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

The following is an examiner's statement of reasons for indicating allowance of claims 12 and 21: The prior art does not disclose a second resistor, a third resistor, and a fourth resistor connected in series coupling the sensing

node to the second input of the comparator; and second operation amplifier having one input connected to a point between the second resistor and the third resistor, another input connected to the circuit ground, and an output connected to another point between the third resistor and the fourth resistor. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

Response to Arguments

4. Applicant's arguments with respect to claims 1 and 7 have been considered but are moot in view of the new ground(s) of rejection.

Applicant comments on pages 2-3 of the Remarks that the prior art does not disclose the step of disconnecting the power source from the load circuits based on a current threshold value that is changed as a function of the voltage applied to the equipment rather than being fixed.

The new reference by Poe et al. [Patent No. 6,646,847] determines the voltage applied to the load, and a current threshold value that is changed based on a voltage applied to the load circuits, and disconnects the power source from the circuits when electric power consumed by the circuits exceeds a threshold level [See above rejections of claims 1 and 7].

Based on examiner's best understanding, it is believed that the prior art reference by Poe and Jones read on the amended claim language of independent claims 1 and 7.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DHP
01/09/2007

Stephen W Jackson 1-10-07

STEPHEN W. JACKSON
PRIMARY EXAMINER